| #1 | #2 | #3 | #4 |
|---|---|---|---|
| | | | |

- Open-book, one 8.5 by 11 inch page of handwritten notes (two sided)
- Write all your work and answers on the exam sheet
- Clearly mark results with a box around them
- Show your work (large and small-signal circuit diagrams, design equations)
- ~~Cross out incorrect answers.~~ If you present two or more inconsistent answers we invariably grade the wrong one.
- All problems have equal weight.
- Notation: $V_x = V_X + v_x$, where $V_X$ is the large signal bias and $v_x$ is the small signal value.
- The math is trivial for all problems, if approached correctly. This is not a course about complicated algebra and calculus! Even I could solve the problems, and I had many years to forget whatever math I learned.

Use the following parameters in all problems, unless otherwise specified:

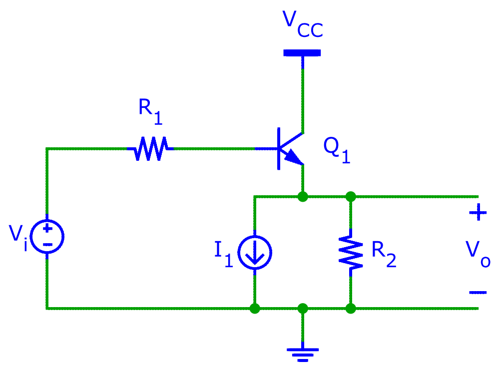
| Device | Parameter values |
|---|---|
| BJT | $I_s = 1\,\text{fA}$, $\beta = 100$, and $V_A = 100\,\text{V}$ |
| NMOS | $\|V_{TH}\| = 400\,\text{mV}$, $\mu_n C_{ox} = 200\,\mu\text{A}/\text{V}^2$, $\lambda = 0.02\,\text{V}^{-1}$, $\gamma = 0\,\text{V}$. |
| PMOS | $\|V_{TH}\| = 400\,\text{mV}$, $\mu_p C_{ox} = \mathbf{100}\,\mu\text{A}/\text{V}^2$, $\lambda = 0.02\,\text{V}^{-1}$, $\gamma = 0\,\text{V}$. |

Unless otherwise specified, assume room temperature and $V_t = 25\,\text{mV}$.

1. Calculate the small-signal output resistance $R_o$ at terminal $V_o$ of the circuit below. The circuit is biased such that the large signal output voltage $V_O = 1\,\text{V}$.

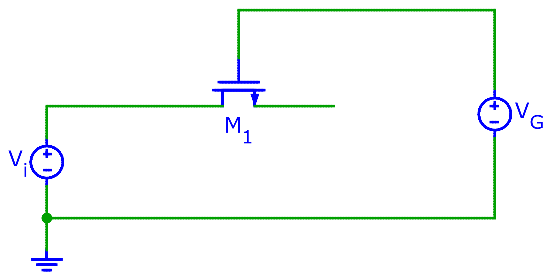
   a) Draw the small-signal model and calculate the numerical values of all small-signal parameters.
   b) Derive an algebraic expression for $R_o$. You may use the shorthand $r_x \parallel r_y$.
   c) Calculate the numerical value of $R_o$.

   Use $V_{cc} = 3\,\text{V}$, $R_1 = 1\,\text{k}\Omega$, $R_2 = 5\,\text{k}\Omega$, $I_1 = 500\,\mu\text{A}$.



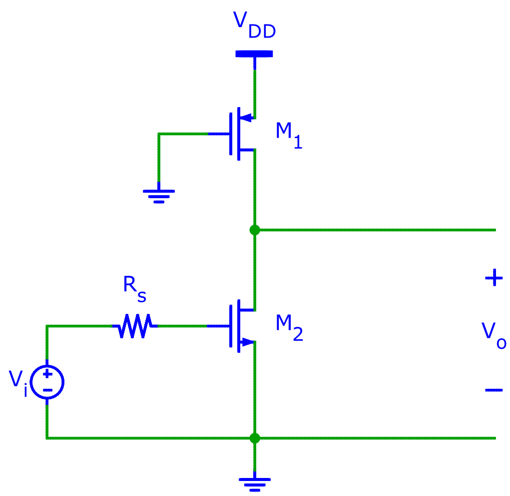
2. Determine the value of $V_G$ such that the channel resistance (resistance between the source and the drain of $M_1$) is $1\,\mathrm{k}\Omega$ for $V_i = 2\,\mathrm{V}$ and $I_D = 0\,\mathrm{A}$.

   Use $W_1 = 2\,\mu\mathrm{m}$ and $L_1 = 180\,\mathrm{nm}$.



3. Analyze the amplifer shown below for $V_{dd} = 3\,\text{V}$, $V_O = V_{dd}/2$, $W_1 = W_2 = 5\,\mu\text{m}$ and $L_1 = L_2 = 350\,\text{nm}$. $M_2$ is biased in saturation.

   a) What is the region of operation of $M_1$?
   b) Draw the small-signal model and calculate the values of all small-signal parameters. Beware: $|V_{DS1}| \not\ll |2(V_{GS1} - V_{TH})|$.
   c) Derive an algebraic expression for the small-signal voltage gain $a_v = v_o/v_i$. You may use the shorthand $r_x \parallel r_y$.
   d) Calculate the value of $a_v$.



4. Design a circuit such that $v_o = r_x i_s$ with $r_x = 10\,\text{k}\Omega \pm 2\,\%$ using a single NPN transistor ($V_A = 0\,\text{V}$) and as many resistors and (ideal) bias sources (current or voltage) as you like (fewer is better and helps avoid mistakes). The value of $R_s$ varies in the range $1 \ldots 10\,\text{M}\Omega$. The source $i_s$ is a reverse biased diode and requires $V_s$ in the range $2\,\text{V} \leq V_s \leq 3\,\text{V}$ to work properly. Stay close to the minimum power dissipation (not more than 2x).

   Use the following sequence (you may need to iterate):

   a) Determine the type of amplifier configuration (CE, CB, CC) best suited for this problem.
   b) Draw a prototype large signal model including all biasing elements. You may need to iterate, e.g. modify or add biasing elements during the design process.
   c) Draw the small-signal diagram and determine the small-signal parameters required to meet the specifications.
   d) Calculate the large signal parameters including the values of all bias sources.
   e) Verify that your circuit meets the specifications. You get points for this, even if you determine that you miss a spec and run out of time (or ideas) for addressing the problem.